

REMARKS

Claims 2-15 and 17-20 remain pending in the present application. Independent claims 3, 14, and 19 have been amended. Support for the amendment to claims 3, 14, and 19 can be found, *inter alia*, in Fig. 4c. The specification has also been amended.

Drawing Objections

The drawings have been objected to for failing to show every feature of the invention. Applicants assert that the objection is now moot given the Applicants amendment to the drawings as attached. Support for the drawing amendment can be found, *inter alia*, on page 4 of the Specification.

Rejections Under 35 U.S.C. § 102

Claims 3, 5, 6, 14 and 15 are rejected under 35 U.S.C. §102(b) as being anticipated by Ozawa et al. Applicants respectfully traverse.

With regard to independent claims 3 and 14, Applicants assert that Osawa et al. fail to disclose a backside of semiconductor chip that includes a solder bonding metal layer in contact with and between the semiconductor chip and a solder film as recited in claim 3. Instead, Osawa et al. disclose embodiments of Figs. 3, 5a-f, 7, 9, 10-12 that do not even include a solder film. The embodiment shown in Fig. 14 discloses a silver paste 42 in contact with and between a semiconductor chip 32-2 and a thermally conductive block 33-2 with a solder layer 144 between the thermally conductive block 33-2 and the heat slug 36. In other words, Fig. 14 discloses a thermal conducting block 33-2 and a silver paste 42 between the semiconductor chip 32-2 and

the solder layer 144. This is not the same as a solder bonding metal layer in contact with and between the semiconductor chip and a solder film as recited in claim 3. For at least this reason, Applicants assert that Osawa et al. fail to disclose each and every element of claims 3 and 14 and respectfully request that the 35 U.S.C. § 102 rejection of claims 3 and 14 be withdrawn.

With regard to claims 5, 6, and 15, Applicants assert that claims 5, 6, and 15 are allowable at least because they depend from one of independent claims 3 and 14 which the Applicants believe have been shown to be allowable.

Rejections Under 35 U.S.C. § 103

Claims 2 and 13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ozawa et al. in view of Haley. Applicants respectfully traverse.

As discussed above, Ozawa et al. fail to disclose a backside of semiconductor chip that includes a solder bonding metal layer in contact with and between the semiconductor chip and a solder film as recited in claim 3.

Haley is directed to a substrate or die coupled to a heatsink. The substrate or die has solder bumps for being directly mounted to a circuit board. A heatsink 104 is coupled to the die 103 using an adhesive (Col. 3, lines 55-58). Haley is silent as to a backside of a semiconductor chip that includes a solder bonding metal layer in contact with and between the semiconductor chip and a solder film as recited in claim 3. Claim 3 is not rendered obvious to one skilled in the art by Ozawa et al. in view of Haley. Claims 2 and 13 are allowable at least because they depend from independent claim 3.

Claim 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Ozawa et al. in view of Furukawa et al. Applicants respectfully traverse.

As discussed above, Ozawa et al. fail to disclose a backside of semiconductor chip that includes a solder bonding metal layer in contact with and between the semiconductor chip and a solder film as recited in claim 3.

Furukawa et al. is directed to a semiconductor device capable of attaining a connection or disconnection between an electrode and another conductive area by use of a simple method when the electrode is formed on the main surface of a semiconductor substrate having an irregular surface portion and a method for manufacturing the semiconductor device (Col. 3, lines 59-65). Furukawa et al. is silent as to a solder film and a solder bonding layer. Therefore, Furukawa et al. can not disclose or suggest a backside of semiconductor chip that includes a solder bonding metal layer in contact with and between the semiconductor chip and a solder film as recited in claim 3. Claim 3 is not rendered obvious to one skilled in the art by Ozawa et al. in view of Furukawa et al. Claim 4 is allowable at least because it depends from independent claim 3.

Claim 7 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Ozawa et al. in view of Takahama et al. Applicants respectfully traverse.

As discussed above, Ozawa et al. fail to disclose a backside of semiconductor chip that includes a solder bonding metal layer in contact with and between the semiconductor chip and the solder film as recited in claim 3.

Takahama et al. is directed to a method of manufacturing an insulation substrate for a semiconductor device using a metal pattern plate. Takahama et al. is silent as to a backside of a semiconductor chip that includes a solder bonding metal layer in contact with and between the

semiconductor chip and a solder film as recited in claim 3. Instead, Takahama et al. merely disclose a front of a semiconductor chip soldered to a circuit pattern (Col. 5, lines 45-50 and Fig. 5). Claim 3 is not rendered obvious to one skilled in the art by Ozawa et al. in view of Takahama et al. Claims 7 is allowable at least because it depends from independent claim 3.

Claims 8 and 9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ozawa et al. in view of Myers et al. Applicants respectfully traverse.

As discussed above, Ozawa et al. fail to disclose a backside of semiconductor chip that includes a solder bonding metal layer in contact with and between the semiconductor chip and a solder film as recited in claim 3.

Myers et al. is directed to an ultra-thick film of copper or silver or other suitable conductor material for use in spreading heat laterally. Myers et al. is silent as to a backside of a semiconductor chip that includes a solder bonding metal layer in contact with and between the semiconductor chip and the solder film as recited in claim 3. Instead, Myers et al. disclose a Sn/Pb layer 28 in contact with the bottom side of a semiconductor chip 26. Claim 3 is not rendered obvious to one skilled in the art by Ozawa et al. in view of Myers et al. Claims 8 and 9 are allowable at least because they depend from independent claim 3.

Claim 10 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Ozawa et al. in view of Jeong et al. Applicants respectfully traverse.

As discussed above, Ozawa et al. fail to disclose a backside of semiconductor chip that includes a solder bonding metal layer in contact with and between the semiconductor chip and a solder film as recited in claim 3.

Jeong et al. is directed to an interconnection substrate having one or more conductive trace layers and one or more insulating layers and also having a first surface and a second surface with a plurality of electrical contacts, opposite to the first surface. One or more metal thermal conductive layers having a first surface and a second surface opposite the first surface and exposed to an exterior are attached to the first surface of the interconnection substrate via the first surface of the metal thermal conductive layers. A through hole region is formed at the interconnection substrate and at the metal thermal conductive layers (Col. 2, lines 40-56). Jeong et al. is silent as to a backside of semiconductor chip that includes a solder bonding metal layer in contact with and between the semiconductor chip and a solder film as recited in claim 3 (See, for example, Jeong et al., Figs. 3 and 8 and the discussions thereof). Claim 3 is not rendered obvious to one skilled in the art by Ozawa et al. in view of Jeong et al. Claim 10 is allowable at least because it depends from independent claim 3.

Claims 11 and 12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ozawa et al. in view of Hawthorne et al. Applicants respectfully traverse.

As discussed above, Ozawa et al. fail to disclose a backside of semiconductor chip that includes a solder bonding metal layer in contact with and between the semiconductor chip and a solder film as recited in claim 3.

Hawthorne et al. is directed to a thin dielectric substrate bearing a plurality of conductive leads with a hole circumscribed by the substrate in which is position a die having pads that are bonded to ends of leads carried by the substrate and projecting in the hole for contact with die pads. Hawthorne et al. is silent as to a solder film and a solder bonding layer. Therefore, Hawthorne et al. can not disclose or suggest a backside of semiconductor chip includes a solder

bonding metal layer in contact with and between the semiconductor chip and the solder film as recited in claim 3. Claim 3 is not rendered obvious to one skilled in the art by Ozawa et al. in view of Hawthorne et al. Claims 11 and 12 are allowable at least because they depend from independent claim 3.

Claims 17 and 19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hawthorne et al. in view of Myers et al. Applicants respectfully traverse.

With regard to claim 19, Applicants assert that both Hawthorne et al. and Myers et al., separately or in any proper combination, fail to disclose a backside of semiconductor chip that includes a solder bonding metal layer in contact with and between the semiconductor chip and a solder film as recited in claim 19. As discussed above, neither Hawthorne et al. or Myers et al., separately disclose a solder bonding metal positioned as in claim 19. Therefore, a combination of Hawthorne et al. and Myers et al. can not possibly disclose a backside of semiconductor chip that includes a solder bonding metal layer in contact with and between the semiconductor chip and a solder film as recited in claim 19. For at least this reason, Applicants assert that claim 19 is allowable and respectfully request that the 35 U.S.C. § 103 of claim 19 be withdrawn.

With regard to claim 17, Applicants assert that it is allowable at least because it depends from claim 19 which the Applicants believe has been shown to be allowable.

Claim 18 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Hawthorne et al. in view of Myers et al. as applied to claim 19, and further in view of Takahama et al. Applicants respectfully traverse.

With regard to claim 18, Applicants assert that both Hawthorne et al. and Myers et al., separately or in any proper combination, fail to disclose, as discussed above, a backside of semiconductor chip that includes a solder bonding metal layer in contact with and between the semiconductor chip and a solder film as recited in claimed 19. As discussed above, Takahama et al. is likewise deficient. Therefore, a combination of Hawthorne et al., Myers et al., and Takahama et al. can not possibly disclose a backside of semiconductor chip that includes a solder bonding metal layer in contact with and between the semiconductor chip and a solder film as recited in claim 19. For at least this reason, Applicants assert that claim 18 is allowable and respectfully request that the 35 U.S.C. § 103 of claim 18 be withdrawn.

Claim 20 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Hawthorne et al. in view of Myers et al. as applied to claim 19, and further in view of Jeong et al. Applicants respectfully traverse.

With regard to claim 20, Applicants assert that both Hawthorne et al. and Myers et al., separately or in any proper combination, fail to disclose, as discussed above, a backside of a semiconductor chip that includes a solder bonding metal layer in contact with and between the semiconductor chip and a solder film as recited in claimed 19. As further discussed above, Jeong et al. is likewise deficient. Therefore, a combination of Hawthorne et al., Myers et al., and Jeong et al. can not possibly disclose a backside of a semiconductor chip that includes a solder bonding metal layer in contact with and between the semiconductor chip and a solder film as recited in claim 19. For at least this reason, Applicants assert that claim 20 is allowable and respectfully request that the 35 U.S.C. § 103 of claim 20 be withdrawn.

CONCLUSION

In view of the foregoing, Applicants submit that claims 2-15 and 17-20 are patentable over the relied upon references, and that the application as a whole is in condition for allowance. Early and favorable notice to that effect is respectfully solicited.

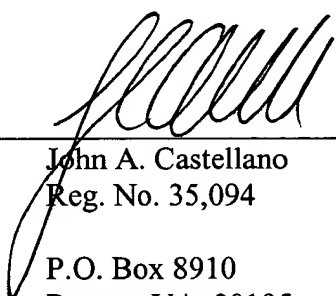
In the event that any matters remain at issue in the application, the Examiner is invited to contact the undersigned at (703) 668-8000 in the Northern Virginia area, for the purpose of a telephonic interview.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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